Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**PAD FUNCTIONS:**

1. **EN**
2. **GND**
3. **VIN**
4. **VOUT**
5. **VOUT**
6. **ADJ**

**.027”**

**4**

**5**

**6**

**3**

**2**

**1**

**.038”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003 X .003”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .027” X .038” DATE: 3/14/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: SIS3950-ADJ**

**DG 10.1.2**

#### Rev B, 7/1